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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,904	10/10/2000	Hironobu Kon	198092US-2S DIV	2551

22850 7590 06/07/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.  
1940 DUKE STREET  
ALEXANDRIA, VA 22314

EXAMINER

FARAHANI, DANA

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AM

<b>Office Action Summary</b>	Application No. 09/684,904	Applicant(s) KON ET AL.	
	Examiner Dana Farahani	Art Unit 2814	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 23-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 23-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 19 July 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.  
     If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some \*    c) ☐ None of:  
         1. ☒ Certified copies of the priority documents have been received.  
         2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
     a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 25-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagisawa et al., hereinafter Yanagisawa (US Patent 5,874,750) in view of Takeda et al. (1200 V Trench gate NPT-IGBT (IEGT) with Excellent Low On-State Voltage, Proceedings of 1998 International Symposium on Power Semiconductor Devices & Ics, Kyoto, pages 75-79.

Regarding claims 25-32, Yanagisawa discloses, referring to figures 3, 4 and 5, an injection enhanced gate transistor made of a semiconductor chip, comprising: a collector electrode formed on the back of the chip 10 (see column 4, lines 43-44); a main emitter, 38 of figure 6, formed on an opposing side of the semiconductor chip; high resistance base layer 33; a gate 35 formed on the opposing side on a channel region between the collector and emitter and a gate insulating film 34 between the channel land gate (Fig. 6); a current sense emitter 12 formed on the opposing side of the semiconductor; current sense terminal ES, wherein electrical current from the collector is made to flow to both the main emitter and the current sense emitter (Fig.3); a plate-like collector electrode terminal 18 arranged on the one side of the power semiconductor device and electrically connected to the collector (Fig.4 and column 4, lines 64-65); a plate-like emitter electrode terminal 16 arranged on the one side of the

power semiconductor device and electrically connected to the emitter (Fig.4, column 4, lines 64-65); wherein the voltage- driven power semiconductor device is a press-contacting type package (see the abstract, lines 1-2).

Yanagisawa does not disclose the gate of the injection enhanced gate transistor being a trench-type gate embedded in the opposing side of the chip, carrier accumulation efficiency of the main emitter and the current sense emitter in On state being greater than that of an insulated gate bipolar transistor (IGBT). However, figure 1 of Takeda et al. shows the gate of the injection enhanced gate transistor being a trench-type gate embedded in the opposing side of the chip, and figures 4 and 5 show carrier accumulation efficiency of the main emitter and the current sense emitter in On-state being greater than that of an insulated gate bipolar transistor in order to offer both sufficient margin for blocking voltage and low on-state voltage Device Design Section, page 75, right column, lines 2-3 from the bottom). It would have been obvious to one having ordinary skill in the art of the time the invention was made to from the gate of the injection enhanced gate transistor being a trench-type gate embedded in the opposing side of the chip and the carrier accumulation efficiency of the main emitter and the current sense emitter in On-state being greater than that of an insulated gate bipolar transistor, as taught by Takeda et al., in the device of Yanagisawa et al., to offer both sufficient margin for blocking voltage and low on-state voltage.

Regarding Claim 33, Yanagisawa in view of Takeda discloses the limitations in the claim, as discussed above, except for expressly disclosing a plurality of chips. It would have been obvious to one of ordinary skill in the art to include additional IEGT

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chips in the device of Yanagisawa in view of Takeda, since it is a customary practice in the art to make a plurality of transistor devices, as a lot of device applications of the transistors use a large number of the transistors. It has been held that duplicating the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

4. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagisawa in view of Takeda as applied to the claims above, and further in view of Horiguchi et al., hereinafter Horiguchi (US Patent 5,910,675).

Yanagisawa in view of Takeda discloses the limitations in the claim, as discussed above, but does not disclose a an emitter current flowing through the current sense emitter to the one of the IEGT's to an external protection circuit , so that an electrical current from the collector is made to flow to the main emitter and current sense terminal.

Horiguchi discloses in figure 1, a protection circuit, wherein the emitter and gate of the transistors 5 and 4, respectively, are attached to the protection diode (circuit) 8. Therefore, it would have been obvious to one having ordinary skill in the art of the time the invention was made to use such a connection to the emitter/gate of the device of Yanagisawa in view of Takeda in order to control the over-current therein.

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**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

*Wael Fahmy*  
*SPE 2814*